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08/965,286	11/06/1997	TAKAYUKI GOMI	P97.2608	3718

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/965,286	GOMI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6,20-25 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,20-25 and 30-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Figure 5 of the present invention depicts a second embedded diffusion laver located within the substrate and does not overlap with the epitaxial laver. The second embedded diffusion laver does not intersects the substrate and does not intersects the epitaxial laver. Therefore, the claimed limitations of a distance between a location of peak impurity concentration within the second embedded diffusion laver and a location where the second embedded diffusion laver intersects the substrate is less than one-half of a distance-between the location of peak impurity concentration and a location where the second embedded diffusion layer intersects the epitaxial laver, as recited in claim 4, is unclear as to what is the distance between a location of peak impurity concentration within the second embedded diffusion laver and a location where the second embedded diffusion laver intersects the substrate.

The claimed limitations of epitaxial impurity concentration at all depths of the second vertical transistor between the surface of the emitter and a position of peak impurity concentration within the second embedded diffusion laver, as recited in claim 21, are unclear as to what is an epitaxial impurity concentration,

which surface of the emitter is being referred and whether concentration at all depths of the second vertical transistor includes all the depths of the second embedded diffusion laver.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Magdo et al. (4,357,622).

Magdo et al. teach in figure 7 and related text a semiconductor device having a first vertical bipolar transistor and a second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor, formed on a P type semiconductor substrate, an N type epitaxial layer formed on the substrate above the datum surface, a first embedded diffusion layer 22 formed as part of a first vertical bipolar transistor in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 18 formed as part of a second vertical type transistor directly on the substrate,

wherein the second embedded diffusion layer 18 having an impurity concentration that is less than an impurity concentration of the first embedded diffusion layer 22, and

wherein a top and a bottom of the second embedded diffusion layer 13 are formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between the top and bottom of the first embedded diffusion layer 22 and a surface of the emitter of the first vertical type bipolar transistor, respectively.

Regarding the claimed limitations of a first vertical bipolar transistor and a second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor, although Magdo et al. do not explicitly disclose a first vertical bipolar transistor and a second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor, these features are inherent in Magdo et al.'s device for the following reasons. The claimed limitations of a first vertical bipolar transistor and a second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor means that the first transistor is a high speed transistor and the second transistor is a high voltage transistor and thus having higher breakdown voltage than the first transistor. Magdo et al.'s structure, which is identical to the claimed structure, comprises first and second embedded diffusion layers in an NPN and a PNP transistors, and thus rendering the first and second transistors as being high speed and high voltage transistors, respectively (see column 1, lines 10-16). This means that the first vertical bipolar transistor and a

second vertical type transistor having a breakdown voltage that is higher than that of the first vertical type transistor, as claimed.

Furthermore, the limitations of a first transistor functioning as a high speed transistor and a second transistor functioning as a high voltage transistor is a functional limitation. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See In re Casey, 152 USPQ 235 (CCPA1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 6, 21-23, 25 and 30-31, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Magdo et al. in view Yamauchi et al. (5,151,765).

Magdo et al. teach in figure 7 and related text substantially the entire claimed structure, as recited in claim 32, except first and second embedded diffusion layers are formed as a part of the respective collector regions. That is, Magdo et al. do not teach a second NPN transistor. Yamauchi teaches in figure 5 and related text a second NPN transistor, wherein first and second embedded diffusion layers 2a, 2b are formed as a part of the respective collector regions 3a, 3b, and connected to collector contact regions 7a, 7b.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second NPN transistor in Magdo et al.'s device, in order to simplify the processing steps of making the device by conventionally reversing the polarity of a transistor. Furthermore, Magdo et al. teach the difficulties of forming a PNP transistor, and that a PNP transistor has inferior characteristics (column 1) in comparison to an NPN transistor. Therefore, one skilled in the art would be motivated to form a second NPN transistor in order to improve the performance of the device and to simplify its fabrication process.

Regarding claims 4 and 21, although figure 10 of Magdo et al. does not depict a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer, at all distances greater than a distance from the surface of the emitter of the second vertical type bipolar transistor to a peak position of the impurity concentration of the second embedded diffusion layer, and epitaxial impurity concentration at all depths of the second vertical transistor between the surface of the emitter and a position of

peak impurity concentration within the second embedded diffusion laver, these features are inherent in Magdo et al.'s device, because it is well known in the art that diffused areas have concentration that follows natural distribution curve, of which official notice is taken (See Watanabe et al., figure 9, graph 22"). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to dope the second embedded diffusion laver such that the distance between a location of peak impurity concentration within the second embedded diffusion laver and a location where the second embedded diffusion laver intersects the substrate is less than one-half of a distance-between the location of peak impurity concentration and a location where the second embedded diffusion layer intersects the epitaxial laver in prior art's device in order to adjust and improve the characteristics of the device.

Regarding claim 6, Magdo et al. teach a second embedded diffusion layer having an impurity concentration of 1E13 to 1E15 (column 4, lines 8-9).

Regarding claim 22, Magdo et al. teach a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the surface of the emitter that is approximately equal to a location of the bottom of the first embedded diffusion layer from the surface of the emitter.

Regarding claim 23, Magdo et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type bipolar

transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Regarding claim 26, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

Regarding claims 30 and 31, the first vertical type bipolar transistor is capable of operating at a higher speed and a lower voltage tan the second vertical type bipolar transistor.

Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magdo et al. and Yamauchi et al., as applied to claim 1 above, and further in view of Kumamaru et al. (4,379,726).

Regarding claims 20 and 24, Magdo et al. teach in figure 7 and related text substantially the entire claimed structure, as recited in claim 32, except first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers to define first and second epitaxial thicknesses, respectively, wherein the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

Kumamaru et al. teach substantially the entire claimed structure, as applied to claim 1 above, including first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers

to define first and second epitaxial thicknesses, respectively, wherein the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers to define first and second epitaxial thicknesses, respectively, wherein the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer in the device of Magdo et al. and Yamauchi et al., in order to improve the characteristics of the device.

Response to Arguments

Applicant argues that Magdo does not teach a first high speed transistor and a second high voltage transistor having higher breakdown voltage than the first transistor.

Magdo et al. teach a semiconductor device having a first vertical bipolar transistor and a second vertical type transistor having first and second embedded diffusion layers in an NPN and a PNP transistors. Magdo et al. further teach that NPN and PNP transistors are high frequency (speed) and low frequency transistors, respectively (see column 1, lines 10-16). Therefore, Magdo et al.

teach a first high speed transistor and a second high voltage transistor having higher breakdown voltage than the first transistor.

Applicant argues that claim 1 does not recite a second NPN transistor, and the examiner must still show first and second embedded diffusion layers are formed as a part of the respective collector regions

Magdo et al. teach an NPN and PNP transistors, wherein the respective collectors are regions 22 (N+) and 38 (P+). Forming a second NPN transistor in Magdo et al.'s device means that the collector is of an N-type (and not of a P type), and therefore the second embedded diffusion layer 18 (of N type conductivity) would be considered as part of the collector (since it has the same conductivity type as that of the collector).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 14, 2004

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800